Claims:

1. A magnetic random access memory (MRAM) comprising:

an array of magnetic memory cells arranged on a cross-point grid in which each memory cell represents a resistive current path;

a plurality of bit and word select lines in said cross-point grid connected to address individual ones of said memory cells, and such lines having stray capacitances on which spurious voltages can build up on unselected ones of said lines; and

a plurality of diodes connected to limit and discharge said spurious voltages on said unselected lines;

wherein, device operating margins are improved.

2. The MRAM of claim 1, wherein:

the array of magnetic memory cells has an increased size made possible by said improved device operating margins.

3. The MRAM of claim 1, further comprising:

a word line decoder connected to the plurality of bit and word select lines and such that unselected ones are high impedance and can build floating voltages that would otherwise disturb said device operating margins.

4. The MRAM of claim 1, wherein:

the plurality of diodes are individually connected between a common voltage reference and independent ones of the plurality of bit and word select

lines, and bleed off excess charges that would otherwise disturb said device operating margins.

5. The MRAM of claim 1, further comprising:

a plurality of current limiting resistors each in series with individual ones of the plurality of diodes, and the series combinations individually connected between a common voltage reference and the plurality of bit and word select lines, wherein bleed off excess charges are bled off that would otherwise disturb said device operating margins.

6. A magnetic random access memory (MRAM) comprising:

an array of magnetic memory cells arranged on a cross-point grid wherein each memory cell represents a resistive current path;

a plurality of word select lines in said cross-point grid connected to address rows of individual ones of said memory cells, and such word lines having stray capacitances on which spurious voltages can build up on unselected ones of said lines; and

a decoder connected to independently drive each one of the plurality of word select lines between ground and a clamping voltage, and not allowing a high impedance state of any of the plurality of word select lines that would otherwise allow floating voltages to build up and disturb said device operating margins.

7. The MRAM of claim 6, wherein:

the array of magnetic memory cells has an increased size made possible by said improved device operating margins.

8. The MRAM of claim 6, further comprising:

a voltage reference connected to the decoder and providing for each word line to assume an equi-potential voltage when not selected.